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Substitute for Form 1449A/PTO  <b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (use as many sheets as necessary)			Complete If Known		
			Application Number	10/661,130	
			Filing Date	9/12/2003	
			First Named Inventor	Visokay et al.	
			Group Art Unit	2825	
Examiner Name	MALSAWMA				
Sheet	1	of	2	Attorney Docket No.	TI-35942

U.S. PATENT DOCUMENTS						
Exam. Initials*	Cite No. <sup>1</sup>	U.S. Patent Document		Name of Patentee or Applicant of Cited Doc.	Date of Pub. of Cited Doc. (mm-dd-yyyy)	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code <sup>2</sup> (if known)			
AM	AA	4,628,588		McDavid	12/16/1986	Entire Document
	AB	4,641,417		McDavid	02/10/1987	Entire Document
	AC	4,672,419		McDavid	06/09/1987	Entire Document
	AD	4,954,867		Hosaka	09/04/1990	Entire Document
	AF	5,633,522		Dorleans et al.	05/27/1997	Entire Document
	AG	5,723,893		Yu et al.	03/03/1998	Entire Document
	AH	5,937,315		Xiang et al.	08/10/1999	Entire Document
	AJ	6,376,342	B1	Tseng	04/23/2002	Entire Document
	AK	6,410,967	B1	Hause et al.	06/25/2002	Entire Document
	AL	6,432,817	B1	Bertrand et al.	08/13/2002	Entire Document
	AM	6,602,781	B1	Xiang et al.	08/05/2003	Entire Document
	AN	6,617,624	B2	Powell	09/09/2003	Entire Document

FOREIGN PATENT DOCUMENTS								
Exam. Initials*	Cite No. <sup>1</sup>	Foreign Patent Document			Name of Patentee or Applicant of Cited Doc.	Date of Pub. of Cited Doc. (mm-dd-yyyy)	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T <sup>6</sup>
		Office <sup>3</sup>	Number <sup>4</sup>	Kind Code <sup>2</sup> (if known)				
	BA							
	BB							
	BF							
	BG							
	BH							

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS			
Exam. Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	† <sup>2</sup>
AM	CA	"An Investigation of Molybdenum Gate for Submicrometer CMOS", ROBERT F. KWASNICK, EDMUND B. KAMINSKY, PAUL A. FRANK, GERHARD A. FRANZ, KENNETH J. POLASKO, RICHARD J. IAJA and THOMAS B. GORDZYA, IEEE Transactions on Electron Devices, Vol. 35, No. 9, September, 1988, pp. 1432-1438.	
AM	CB	"Silicon Processing for the VLSI Era, Volume 2: Process Integration", STANLEY WOLF, Ph.D., Copyright, 1990 by Lattice Press, 7 pgs.	
AM	CC	"Electrical Characteristics of TiB <sub>2</sub> for ULSI Applications", CHANG SIK CHOI, QINGFENG WANG, CARLTON M. OSBURN, GARY A. RUGGLES and AYAN S. SHAH, IEEE Transactions on Electron Devices, Vol. 39, No. 10, October, 1992, pp. 2341-2345.	
Examiner Signature		<i>AM Malbran</i>	Date Considered 7/28/04

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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Other Prior Art/Non-Patent Literature Documents: <sup>1</sup>Unique citation designation number. <sup>2</sup>Applicant is to place a check mark here if English Translation is attached.

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Sheet	2	of	2	Attorney Docket No.	TI-35942

CD	"FinFET Process Refinements for Improved Mobility and Gate Work Function Engineering", YANG-KYU CHOI, LELAND CHANG, PUSHKAR RANADE, JEONG-SOO LEE, DAEWON HA, SRIRAM BALASUBRAMANIAN, ADITYA AGARWAL, MIKE AMEEN TSU-JAE KING and JEFFREY BOKOR, IEEE, 2002, 4 pgs.
CE	"MO <sub>2</sub> N/Mo GAFF MOSFETs". MANJIN J. KIM and DALE M. BROWN, IEEE, 1982, 4 pgs.
CF	"Application of MoSi <sub>2</sub> to the Double-Level Interconnections of i <sup>2</sup> L Circuits", YOSHITAKA SASAKI, OSAMU OZAWA and SHUICHI KAMEYAMA, IEEE Transactions on Electron Devices, Vol. ED-27, No. 8, August, 1980, 5 pgs.
CG	"Work Function Controlled Silicide Technology for Submicron CMOS", MASAKAZU KAKUMU and KAZUHIKO HASHIMOTO, No source or date available, 2 pgs.
CH	"Refractory Metal Silicide/N <sup>+</sup> Polysilicon in CMOS/SOS", B. C. LEUNG and J.S. MAA, No source or date available, 4 pgs.
CI	"Fabrication of Mo-Gate/Ti-Silicide-Clad-Moat MOS Devices by Use of Multilayer-Glass Depositions", J. M. MCDAVID, IEEE Electron Device Letters, Vol. EDL-5, No. 9, September, 1984, 2 pgs.
CJ	"Lightly Impurity Doped (LD) Mo Silicide Gate Technology", MASAKAZU KAKUMU and JUN'ICHI MATSUNAGA, IEEE, 1985, 4 pgs.

Examiner Signature	<i>S. Malawma</i>	Date Considered	7/28/04
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\* These references not considered because their sources/dates are not provided.